Development of a Single Stage C-Band Pulsed Power Amplifier for RADAR Transmitter

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Abstract— **This paper presents the design and development of a single stage solid state pulse power amplifier (SS-PPA) working at 7.23 GHz ± 100 MHz frequency by using hybrid technology. The amplifier is designed to achieve maximum power gain with medium output power by adopting simultaneous conjugate matching procedure. Commercial available packaged pseudomorphic high electron mobility transistor (pHEMT) FPD6836P70 (from RFMD) is used for designing the amplifier. A pulse aggregate card has been developed to provide pulse bias. Plated through hole (PTH) technique is used for good high frequency grounding. At room ambient temperature, the measured peak output power from the prototype amplifier is 18.31 dBm for 8 dBm input driving power, measuring 10.31 dB gain. We present a description of the design of the amplifier, its simulated and measured results and their comparison with desired specifications.** *(Abstract)*

Keywords-pulse power amplifier; peak power; pulsed RF; rise/fall time; pulse repetition frequency; distributed matching networks (keywords)

I. INTRODUCTION

Medium to high power microwave pulses are used in a number of applications including pulsed radar [1], medical electronics [2], communication system [3] etc. However, in moving target indicator (MTI) and tracking radar applications, short pulses with low pulse repetition frequency (PRF) are desired to avoid ambiguities in range (no multiple time-around echoes) [4]. Thus pulse power amplifier (PPA) with very low duty cycle is one of the important components in the transmitter chain of the radar front-end. And for short pulse radar, rise and fall time plays critical factor; to be as small as possible.

This paper presents the design and fabrication of a single stage solid state pulse power amplifier working at 7.23 GHz ± 100 MHz frequency. This amplifier can well be used as the first stage of a two stage pulsed power amplifier. The frequency is selected based on the fact that its output can be multiplied (by putting ×13 frequency multiplier) to obtain 94 GHz pulsed radar signal.

The circuit design starts from the selection of proper active device for the frequency band of interest, stability analysis, matching circuits, circuit simulation and optimization, pulse bias technique etc. For design and simulation purpose, Advanced Design System (ADS-2008, update 2) provided by Agilent Technologies, is used. The circuit is fabricated and discrete components are mounted by hybrid microwave integrated circuit (MIC) technology. Finally the results are measured using the Agilent Technologies' PSG series signal generator (E-8257D) and PSA series spectrum analyzer (E-4446A).

The rest of the paper is organized as follows: Section II provides the amplifier detailed design procedure including desired specifications. Circuit fabrication and assembly process along with the components and substrate material used is discussed in section III. Section IV describes the overall measurement procedure and experimental results for the prototype amplifier. Finally we conclude in section V.

II. AMPLIFIER DESIGN

An amplifier design starts by reviewing its specifications for overall performance. High peak power and small rise (T_r)/ fall (T_f) time are the important requirements for designing a short pulse power amplifier. Table I gives the desired target specifications for the PPA:

TABLE I. DESIGN SPECIFICATIONS

Parameter	Specification
Operating Frequency	7.23 GHz
Band Width	200 MHz
Peak Output Power	20 dBm
Input Driving Power	(7-9) dBm
Pulse Width	(80-120) ns
Rise/Fall Time	≤ 10 ns
Pulse Repetition Frequency (PRF)	30 KHz
DC Power Requirement	+12 V,10 mA/ -12 V, 50 mA
Input/output Connector	50Ω SMA

A. Active Device Selection

Power amplifiers are characterized by parameters such as power compression, intermodulation distortion (IMD), power added efficiency (PAE) etc. At microwave frequencies, the most mature technology for this purpose is metal semiconductor field effect transistor (MESFET). However, for pulsed power amplifier with narrow pulse width and small rise/fall times, the device cut-off frequency has to be high, which require small gate length that translates to smaller channel thickness. This imposes higher doping in order to conserve drain- source current (I_{ds})

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performance and thus smaller breakdown and power [5]. This puts the limitation of MESFET to be used for narrow pulse width applications. But for pHEMT, active channel and doping layer are separate, hence cut-off frequency is higher. Therefore, pHEMTs are mostly used for high speed, high efficiency and high frequency (millimeter wave) applications [6, 7]. "Fig. 1" summarizes the power performance of pHEMTs, MESFETs and HBTs (constituting of different materials) versus frequency.

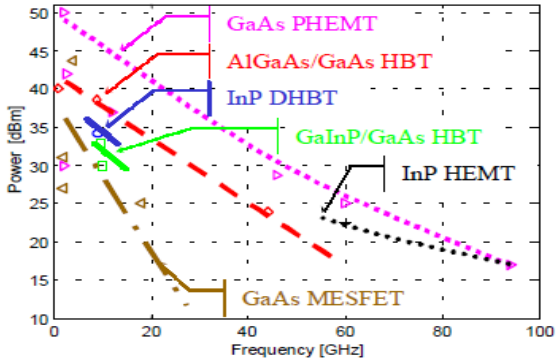

Figure 1. Power performance of MESFETs, HEMTs and HBTs as a function of frequency [5]

For this design, RFMD's (Filtronic) packaged pHEMT (FPD6836P70) has been chosen [8]. This selected surface mountable, low parasitic packaged depletion mode AlGaAs/InGaAs Schottky Barrier gate pHEMT is optimized for high frequency, high speed and low noise applications. This device provides 22 dBm power at 1 dB gain compression for V_{DS} = 5 V and I_{DS} = 55 mA (corresponding V_{GG} = -0.45 V). Its nonlinear model and external package parasitic parameters of this active device are included in TriQuint TOM3 Scalable Nonlinear FET Model in ADS for simulation works.

B. Pulsing Technique of pHEMT Amplifiers

With an applied CW RF drive, pulsed output from a solid state pHEMT amplifier can be obtained in one of the following two ways [9]:

- Switching the gate voltage between a low negative voltage which results in efficient RF power amplification and a higher negative voltage near the pinch off voltage which effectively turns off the drain current (gate pulsing technique).
- Switching the drain voltage between the levels needed for efficient power amplification and zero volts (drain pulsing technique).

In gate pulsing technique, due to thermal effects, no significant improvement in power performance over CW conditions is reported [10]. Besides, with the presently available devices, which lack ideal gate control and pinch off, there is leakage in 'off' state, therefore significant output power in off state. On the other hand, in pulsed drain operation, due to high currents being switched, switching speeds are somewhat slower. Table II summarizes the relative merits and demerits of both the techniques.

For the specified pulse width, drain pulsing technique is used because it is more efficient, provides simpler biasing circuit and very high peak to off state power ratio [11]. "Fig. 2" illustrates the schematic diagram of drain pulsing technique used in the design.

TABLE II. GATE AND DRAIN PULSING COMPARISON

Pulsing Technique	Gate Pulsing	Drain Pulsing
Merits	▪ Narrow pulse width achievable ▪ Faster switching speed	▪ High efficiency ▪ Higher peak power ▪ Very small RF leakage power ▪ Simpler biasing circuit
Demerits	▪ Peak output power not much improved than CW power ▪ Low efficiency	▪ Slower switching speed ▪ Difficult to achieve very narrow pulse width

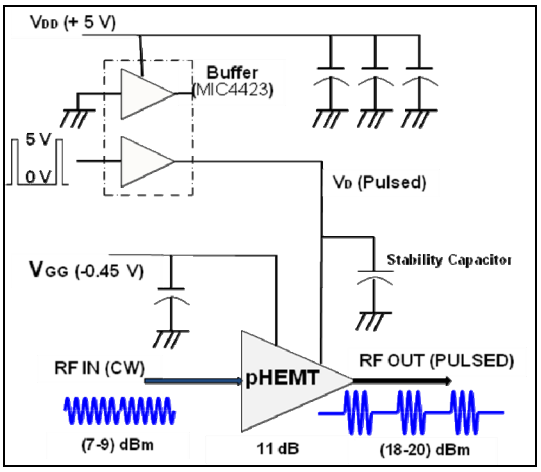

Figure 2. Schematic diagram for drain pulsing

C. Impedance Matching Networks

From the S-parameters provided in the datasheet of pHEMT, it is calculated and estimated that the device is unconditionally stable for the frequency band selected (Δ<1, K>1). Therefore any source and load impedance will result stable operation. Since the amplifier is designed to achieve maximum available power gain with medium output power, simultaneous conjugate matching technique is used. The following formulae are used for calculating source and load impedances [12]:

$$\Gamma_s = \Gamma_{in}^*, \Gamma_L = \Gamma_{out}^*$$

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \qquad \Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s}$$

Considering bilateral Case ($S_{12}\neq 0$), for simultaneous conjugate matching:

$$\Gamma_{Ms} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \qquad \Gamma_{ML} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}$$

Where

$$B_1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2$$

$$B_2 = 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2$$

$$C_1 = S_{11} - \Delta S_{22}^*$$

$$C_2 = S_{22} - \Delta S_{11}^*$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

From the s-parameters provided in the datasheet, the calculated source (Γ_{MS}) and load reflection (Γ_{ML}) coefficients (corresponding impedances) at 7.25 GHz are Γ_{MS}= 0.484<-172.9 (17.4-j2.7 Ω) and Γ_{ML}= 0.297<112.3 (37.4+j20.9 Ω) respectively. This source and load impedances are matched to characteristic impedance (50 Ω) by using microstrip lines as matching elements.

D. *Simulated Results*

The layout of the single stage PPA including the input and output matching networks implemented with distributed microsrip line is shown in "Fig. 3". To reduce the size of the circuit, low impedance shunt stubs and high impedance series stubs has been chosen. Instead of using lumped components, the bias decoupling network is designed by using a high impedance quarter wavelength transmission line and radial stubs. A 30Ω resistor is included in gate bias decoupling circuit to limit the gate current and also increases low frequency stability. Plated through holes (PTH) are used to obtain good high frequency grounding of the transistors.

"Fig. 4" shows the electromagnetic co-simulation results of the layout with real components. From the simulation results, 20.49 dBm peak output power is obtained for 9 dBm driving power. RF leakage in off- state is -7.24 dBm; therefore peak to off state power ratio is more than 27 dB. Simulated input return loss (approximately 20 dB) and output return loss (approximately 10 dB) are shown in "Fig. 5" and "Fig. 6" respectively.

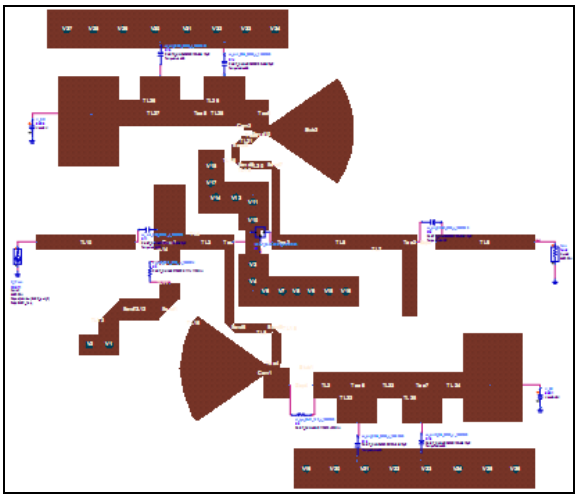

Figure 3. Layout of the single stage PPA

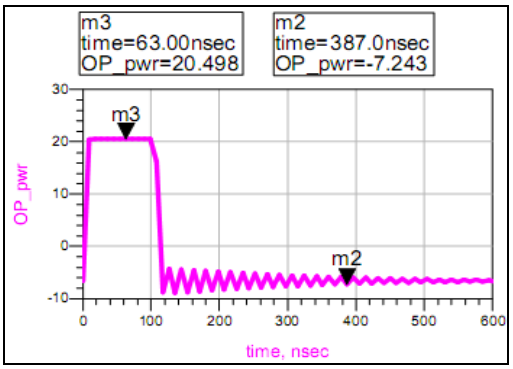

Figure 4. Simulated peak power and leakage power for 9 dBm input drive

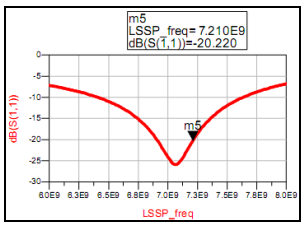

Figure 5. Input return loss

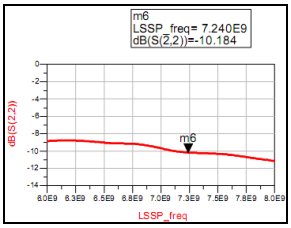

Figure 6. Output return loss

III. FABRICATION AND ASSEMBLY

The circuit was fabricated using Rogers RT/Duroid 5880 [13] double layer substrate material for its low dielectric loss at high frequency. The substrate parameters are presented in Table III.

TABLE III. SUBSTRATE PARAMETERS

Parameter	RT/Duroid 5880
Dielectric constant	2.20±0.02
Substrate thickness	0.254 mm
Metal	Copper
Metal thickness	35 µm
Surface roughness	0.001 mm

The fabricated prototype PPA mounted in aluminum box is shown in "Fig. 7". The pHEMT is bonded with the circuit by using silver filled conductive epoxy (H20E from Epoxy Technologies). All other discrete components and SMA connectors are soldered directly on the substrate.

IV. MEASUREMENTS AND RESULTS

Since the used pHEMT is depletion mode type, it is required to provide negative gate voltage before drain voltage appears. To ensure this voltage sequencing and also to provide pulsed drain modulation, a pulse aggregate card has been developed. It is designed to handle a pulse width of 80 ns-1 µs with 20 µs-1ms pulse repetition interval (PRI).

Typical rise/fall times are <25 ns for 1800 pF capacitive load.

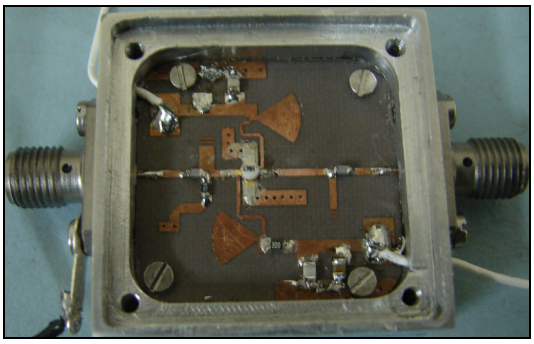

Figure 7. Prototype amplifier housed in Aluminum box

The PPA has been first tested for stable bias point. This is carried out by first applying bias voltages only. "Fig. 8" indicates that the modulation pulse width to the drain terminal of the amplifier is about 106 ns with rise/fall time of 9.5/8.0 ns illustrating pulse aggregate card's switching speed.

Once stable bias point achieved, CW RF drive is applied to the input from signal generator (Agilent Technologies, PSG Series, Model- E-8257D) and "Fig. 9" illustrates the line spectrum presentation of pulsed RF output signal for 8 dBm of CW input power. The line spectrum is the actual Fourier representation of pulsed RF signal in frequency domain. In our measurement, it is obtained by keeping spectrum analyzer's (Agilent Technologies' PSA series model-E-4446A) resolution bandwidth as 3.9 kHz (should be less than 0.3 x PRF). Here the fully resolved each spectral component represents a fraction of the pulse power and the peak power is calculated from the main lobe power by the following formula:

Peak power = main lobe power – pulse desensitization factor, where pulse desensitization factor (α_L) = 20 log (duty factor). Here duty factor = Pulse Width (PW) × Pulse Repetition Frequency (PRF) = 106 ns × 30 kHz = 3.18×10^{-3}. Therefore, $\alpha_L = 20 \log (3.18 \times 10^{-3}) = -49.95$ dB. Here main lobe power is -31.64 dBm, hence peak power is 18.31 dBm (for 8 dBm input power).

This power is calculated without considering cable loss of 0.43 dB at 7.23 GHz. The RF power during off state is -9.14 dBm indicating more than 27 dB peak-off state power ratio.

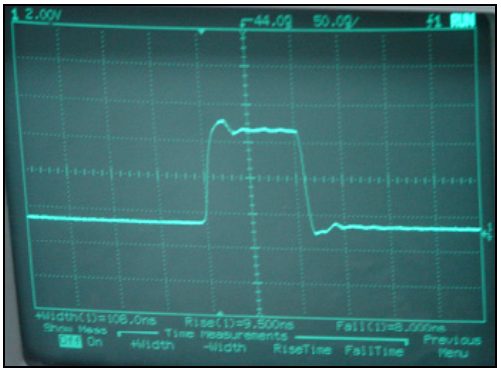

Figure 8. Modulation control pulse

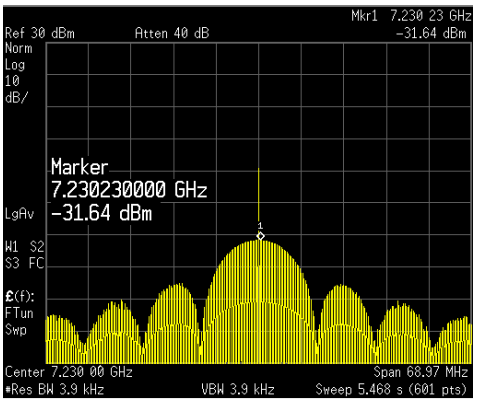

Figure 9. Line spectrum of PPA for 8 dBm input power

V. CONCLUSION

A single stage solid state pulse power amplifier working at 7.23 GHz ± 100 MHz frequency is presented.The measured peak output power from the prototype is 18.31 dBm for 8 dBm driving input power indicating 10.31 dB gain (without considering 0.43 dB cable loss). The measured results are in good aggrement with simulated results and also with the desired target specifications. This prototype amplifier can satisfactorily be used as the first stage of a two stage solid state pulse power amplifier for pulsed radar applications requiring small duty cycle.

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